

FEATURES

- 5 dB NF
- E2-band coverage
- 24 dBm OIP3
- 23 dB gain

TYPICAL APPLICATIONS

- Point-to-point communication
- Instrumentation
- Fiber over radio
- 77 GHz radar

DESCRIPTION

gANZ0033 is a Low Noise Amplifier (LNA) in the E2 (81-86 GHz) frequency band suitable for point-to-point communication. The LNA features 5 dB Noise Figure and very flat frequency response. Furthermore, the LNA has high gain, high linearity and low input/output return loss.

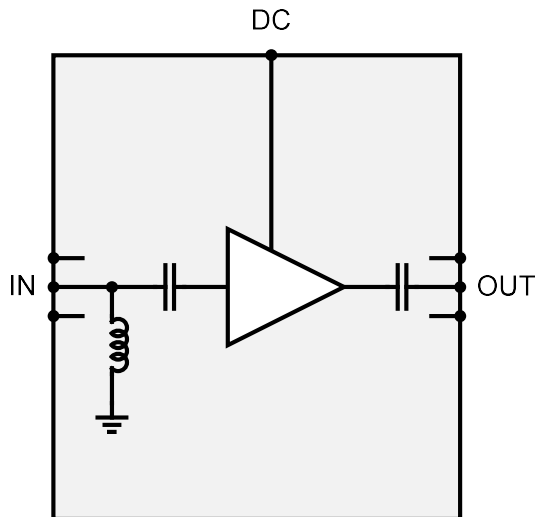


Figure 1. Block diagram of the LNA.

ELECTRICAL PERFORMANCE

Table 1. Electrical performance $T_A=25^\circ\text{C}$

Parameter	Min	Typ	Max	Unit
Frequency	81 (77)		86	GHz
Gain	21	23	25	dB
NF		5		dB
P1dB	9	10	11	dBm
PSAT	12	13	14	dBm
OIP3	19	20	21	dBm
PAE				%
Input return loss	10			dB
Output return loss	15			dB
Power consumption		142		mW

MEASURED PERFORMANCE

The chip has been measured on-wafer using CW and 2-tone input test signals. The LNA uses typical bias settings if not specified differently.

Table 2. Test conditions

Parameter	Setting
RF input power	-25 dBm/tone
RF input frequency	83.5 GHz
Frequency separation	10 MHz
Temperature	25°C

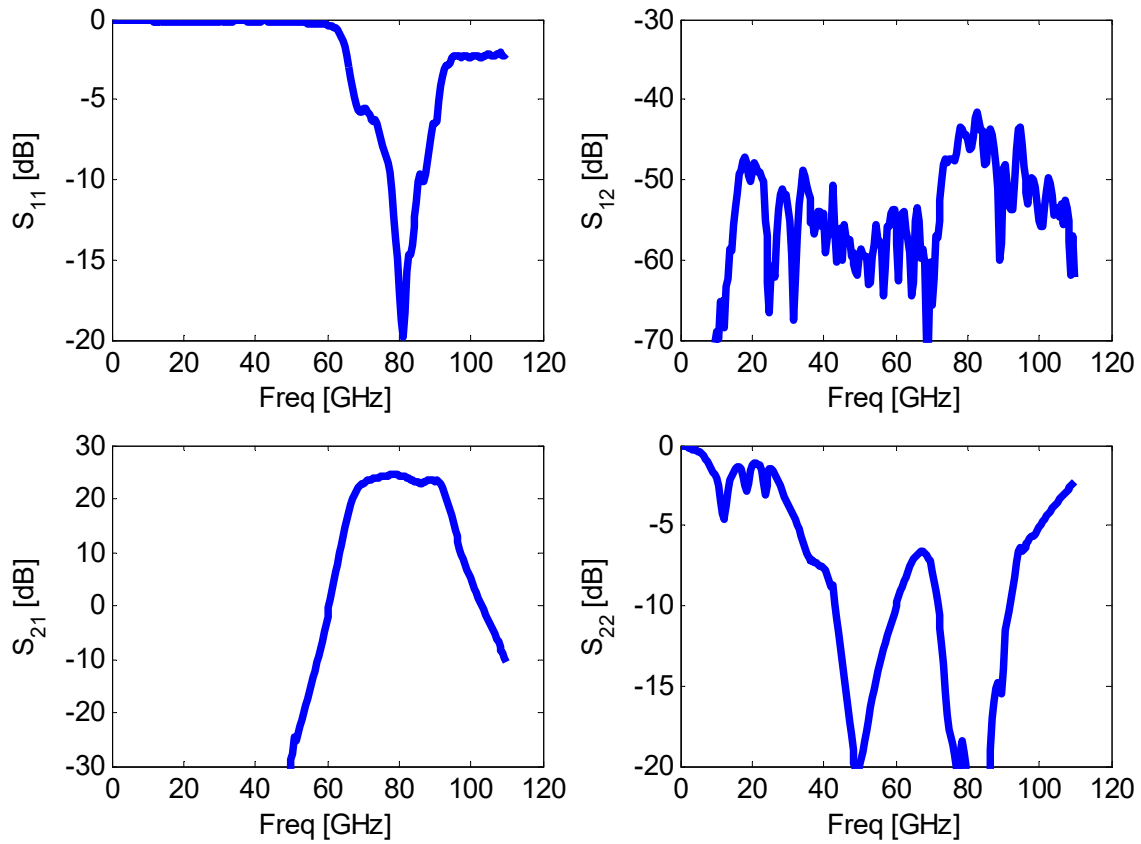
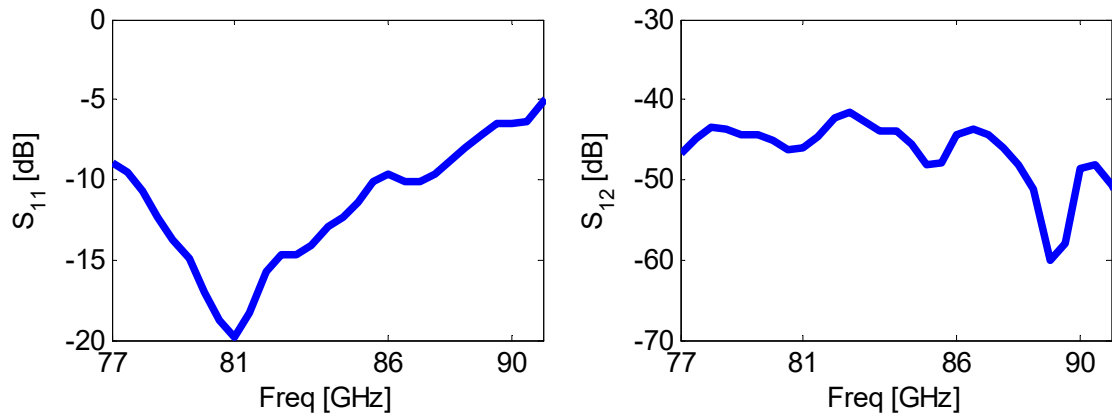


Figure 2. Small signal response from 0-120 GHz at nominal bias. (Upper left): Input matching. (Upper right): Reverse isolation. (Lower left): Small-signal gain. (Lower right): Output matching.



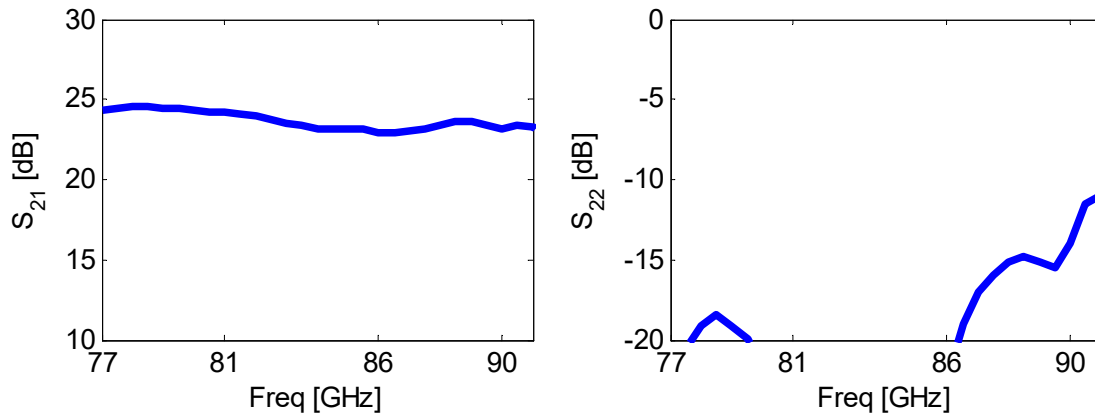


Figure 3. Small signal response within the E2-band at nominal bias. (Upper left): Input matching. (Upper right): Reverse isolation. (Lower left): Small-signal gain. (Lower right): Output matching.

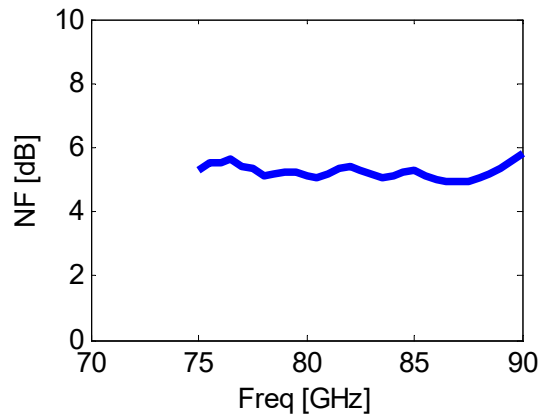


Figure 4. : NF vs freq.

RECOMMENDED OPERATING CONDITIONS

Bias should first be applied to the gates (VG...) followed by the drains (VD...). The gate voltages must be adjusted within the min/max range indicated in Table 3-5 to obtain the specified drain currents. The drain currents are stated with no input signal.

Table 3. Electrical settings on connector P1

Connector P1	Pad No.	Bias settings (V/mA)			I/O
		Min	Typ	Max	
NC	1				NC
VD2	2	1.9	2.0 / 65	2.1	Input
VG2	3	-0.7	-0.5	-0.3	Input
GND	4				Ground
VD1	5	1.1	1.2 / 10	1.3	Input
VG1	6	-0.7	-0.5	-0.3	Input
NC	7				NC

Table 4. Electrical settings on connector P2

Connector P2	Pad No.	Interface	I/O
GND	1		Ground
RF_OUT	2	$Z_0 = 50 \text{ Ohm}$, AC coupled	Output
GND	3		Ground

Table 5. Electrical settings on connector P3

Connector P3	Pad No.	Interface	I/O
GND	1		Ground
RF_IN	2	$Z_0 = 50 \text{ Ohm}$, AC coupled	Input
GND	3		Ground

ABSOLUTE MAXIMUM RATINGS

Table 6. Absolute maximum ratings

Gate-source voltage	-2 to +0.7 V
Drain-source voltage	4.5 V
Gate-drain breakdown voltage	8 V
ID2	120 mA
ID1	50 mA
RF input power	+15 dBm
Operating temperature	-40 to + 85°C
Storage temperature	-65 to +150°C

OUTLINE DRAWING

Mechanical drawing with pad locations is also available in dxf-file format on the web. The substrate thickness is 50 μm (GaAs).

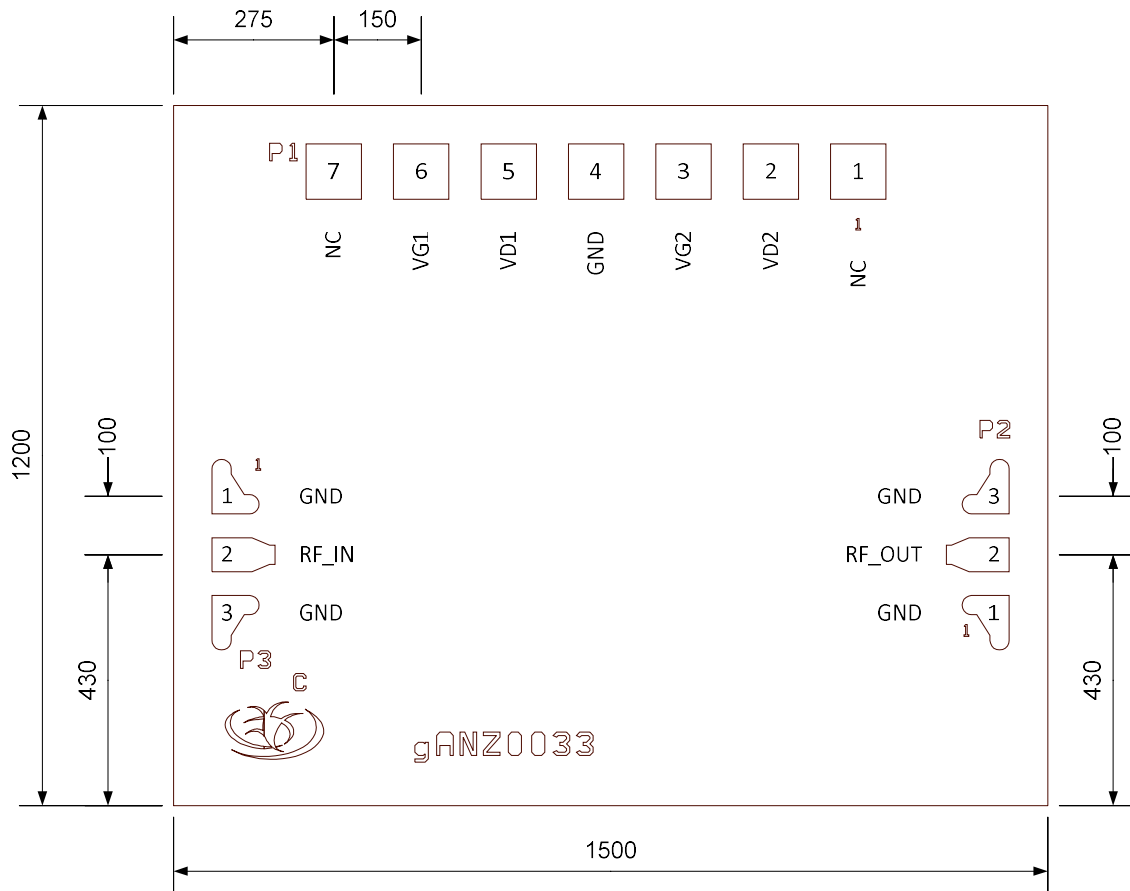


Figure 5. Outline drawing of the MMIC. Dimensions are in μm .