

## FEATURES

- Full E-band coverage
- 21 dB conversion gain
- 25 dB gain control range
- 16/26 dBm P1dB/OIP3
- Direct conversion or IF up conversion

## DESCRIPTION

gTSC0023 is a complete highly integrated transmitter for E-band radio applications. The transmitter offers more than 25 dB gain control (from the VGA and MPA) to compensate for temperature dependent gain variations. The transmitter has a  $\times 6$  frequency multiplier, IQ mixer, VGA, power amplifier and envelope/power detector integrated on the chip. The differential IQ mixer is highly linear with low conversion loss. The frequency multiplier has low spurious and flat output power throughout the entire E-band. The medium power amplifier (MPA) at the output delivers more than 16 dBm (P1dB) output power. The output envelope/power detector can be used for both power and envelope tracking thanks to its wide output bandwidth. The TSC0023B is suitable for wideband high modulation Gbit/s communications.

## TYPICAL APPLICATIONS

- E-band point-to-point radio
- Active imaging
- Automotive radar
- Fiber over radio

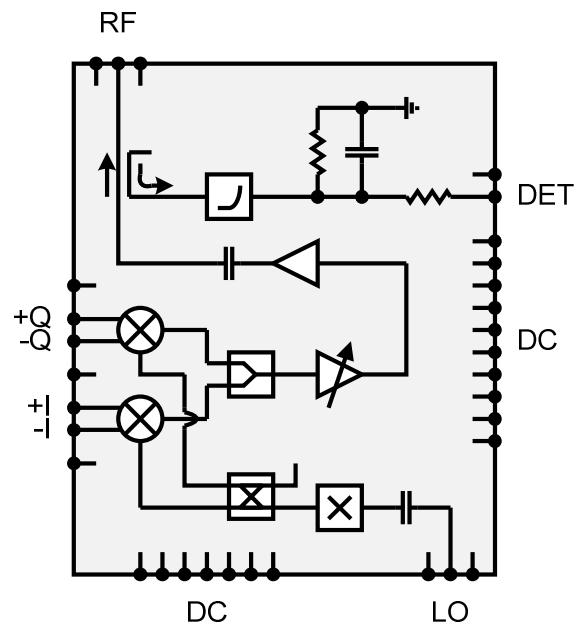


Figure 1. Block diagram of the transmitter.

## ELECTRICAL PERFORMANCE

Table 1. Electrical performance  $T_A=25^\circ\text{C}$

Parameter	Min	Typ	Max	Unit
RF frequency	71		86	GHz
IF frequency	DC		12	GHz
LO input frequency	11.8		14.3	GHz
LO input power	8	10	12	dBm
LO multiplication factor		6		
Max conversion gain <sup>[1]</sup>	18	21	23	dB
Gain control range	25			dB
LO to RF suppression <sup>[2]</sup>	40	45		dBc
Image rejection ratio (IRR)	20			dB
P1dB <sup>[3]</sup>	14	16	18	dBm
PSAT <sup>[3]</sup>	17	19	21	dBm
OIP3 <sup>[3]</sup>	24	26		dBm
OIP2 <sup>[2,3]</sup>	40	50		dBm
Out of band spurioses			-40	dBm
RF return loss	8	10		dB
LO return loss	10	14		dB
Power consumption	1100	1200	1500	mW

## MEASURED PERFORMANCE

The chip has been measured on-wafer using CW and 2-tone input test signals. The transmitter uses typical bias settings if not specified differently.

Table 2. Test conditions

Parameter	Setting
IF input power	-13 dBm/tone
IF input frequency	1 GHz
Frequency separation	10 MHz
Temperature	25°C

<sup>[1]</sup> Gain temperature coefficient is -0.05 dB/°C.

<sup>[2]</sup> Apply I+, I-, Q+ and Q- DC offset voltage for LO cancellation.

<sup>[3]</sup> At maximum gain. VGA drain current (ID1\_VGA+ID2\_VGA) = 100 mA.

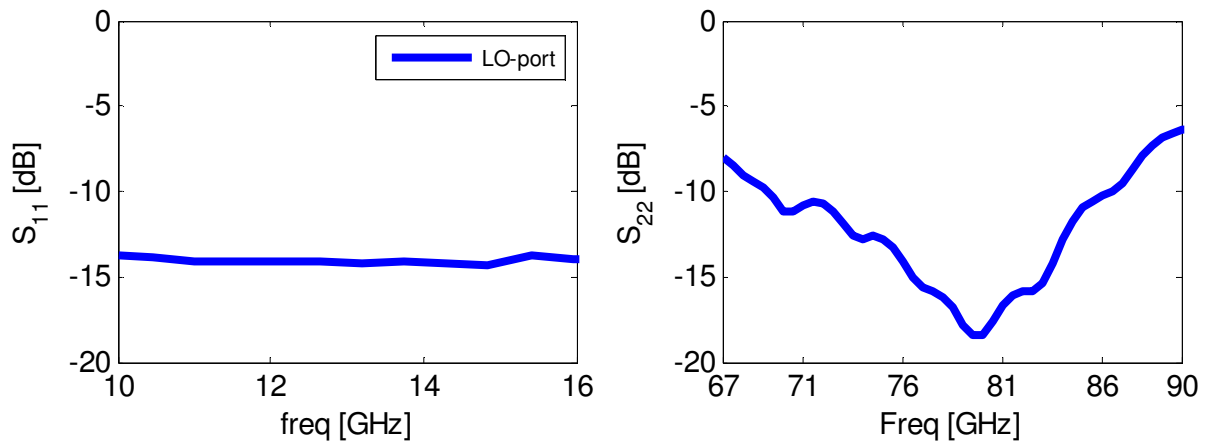


Figure 2. (Left): Input matching of the LO-port. (Right): Output matching of the PA.

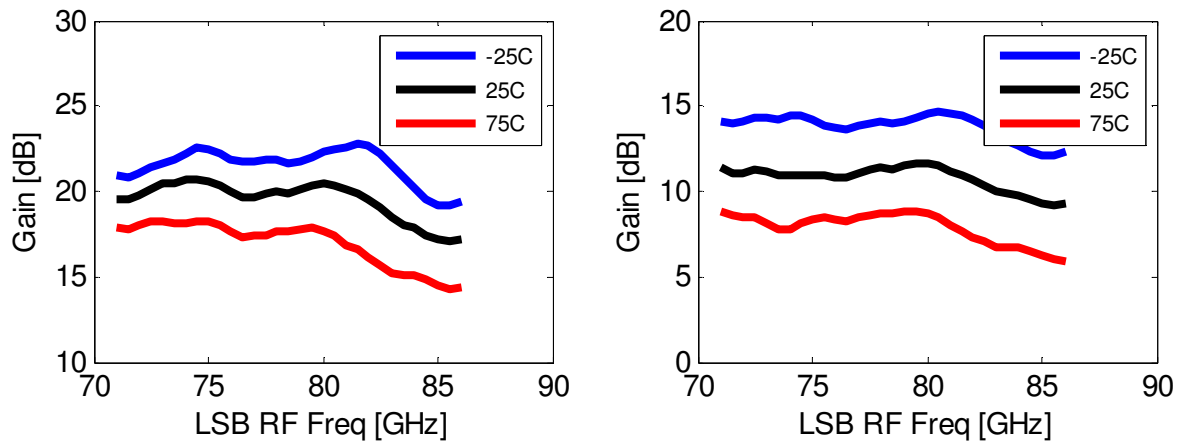


Figure 3. (Left): Maximum conversion gain vs frequency (ID1\_VGA + ID2\_VGA is 100 mA). (Right): Intermediate conversion gain vs frequency (ID1\_VGA + ID2\_VGA is 15 mA).

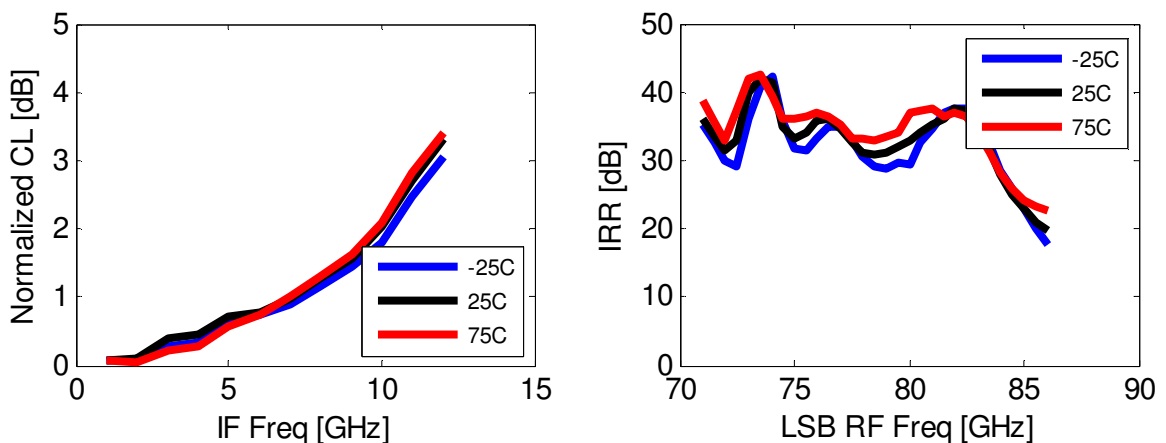


Figure 4. (Left): IF BW measured at a fixed RF frequency of 71 GHz (Right): IRR vs frequency. (ID1\_VGA + ID2\_VGA is 100 mA).

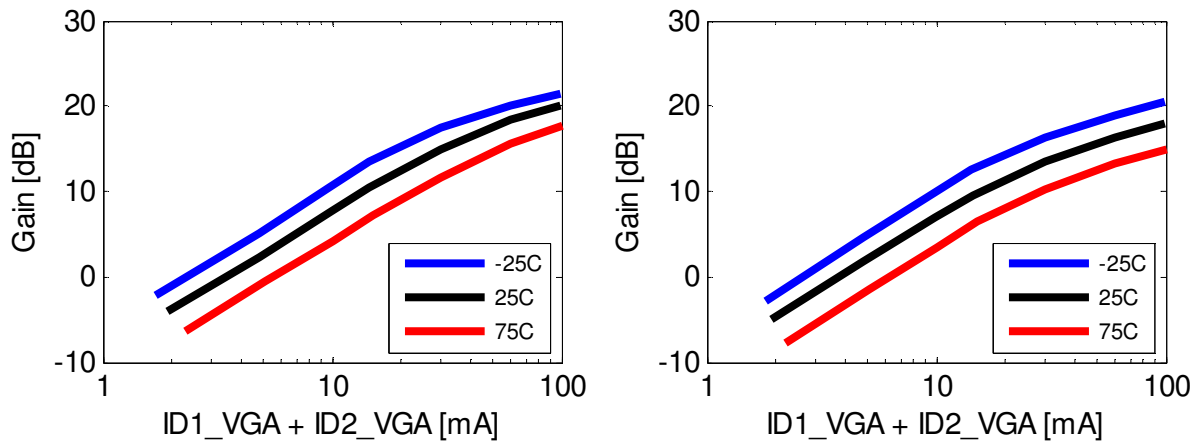


Figure 5. (Left): Gain vs VGA drain current, measured at 73.5 GHz. (Right): 83.5 GHz.

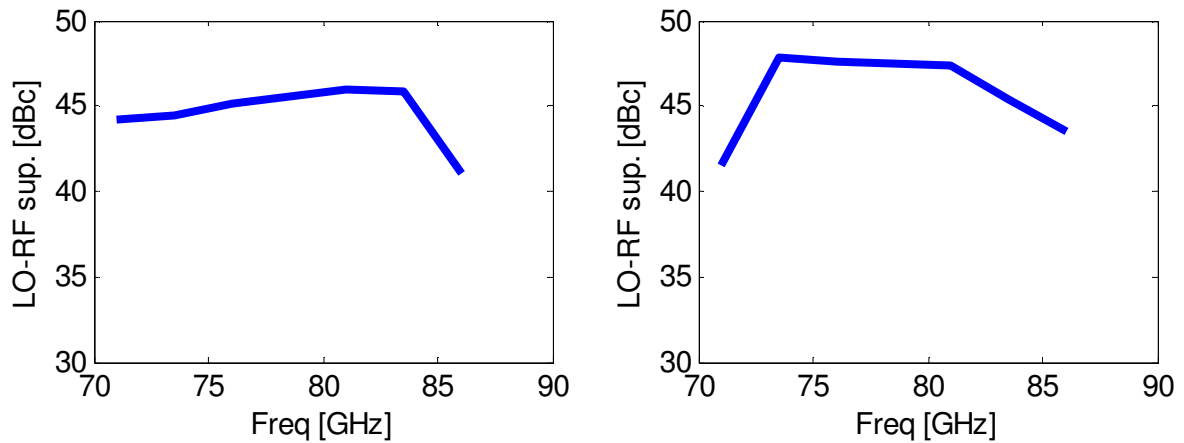


Figure 6. (Left): LO to RF suppression at maximum gain (ID1\_VGA + ID2\_VGA = 100 mA). (Right): LO to RF supr. at intermediate gain (ID1\_VGA + ID2\_VGA = 15 mA). IQ DC offset is applied to cancel the LO.

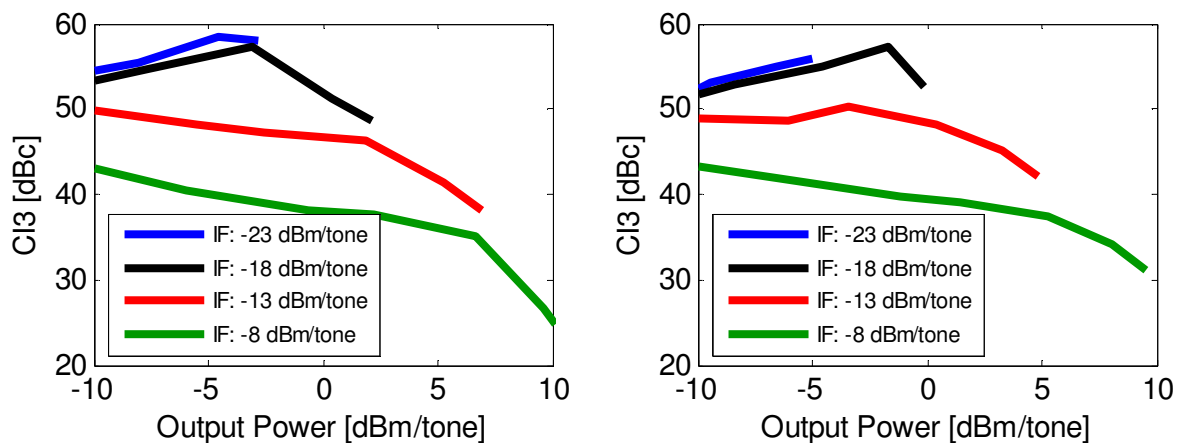


Figure 7. (Left): Third order intermodulation measured at 73.5 GHz, while varying the gain of the VGA to adjust the output power level. (Right): Measured at carrier frequency 83.5 GHz.

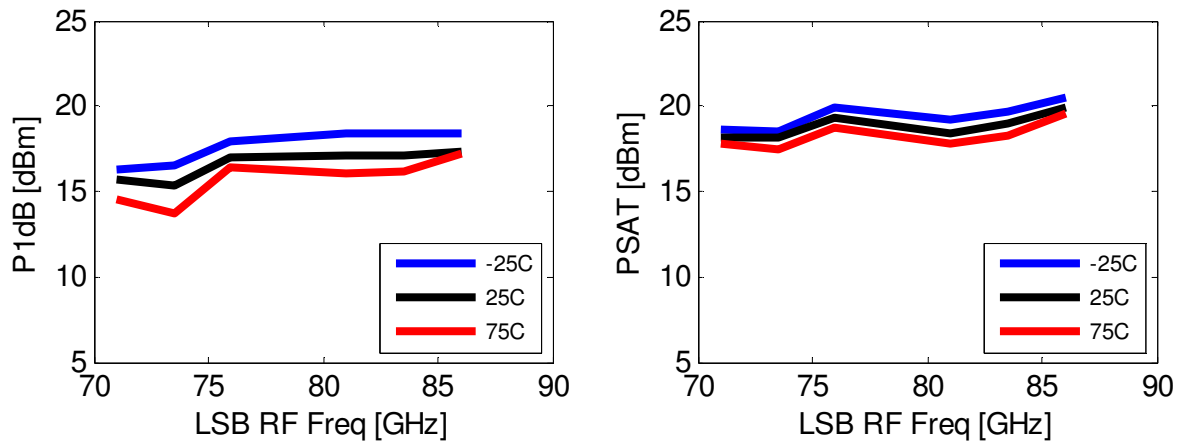


Figure 8. (Left): P1dB at max gain vs freq. (Right): PSAT at max gain vs freq. (ID1\_VGA + ID2\_VGA is 100 mA)

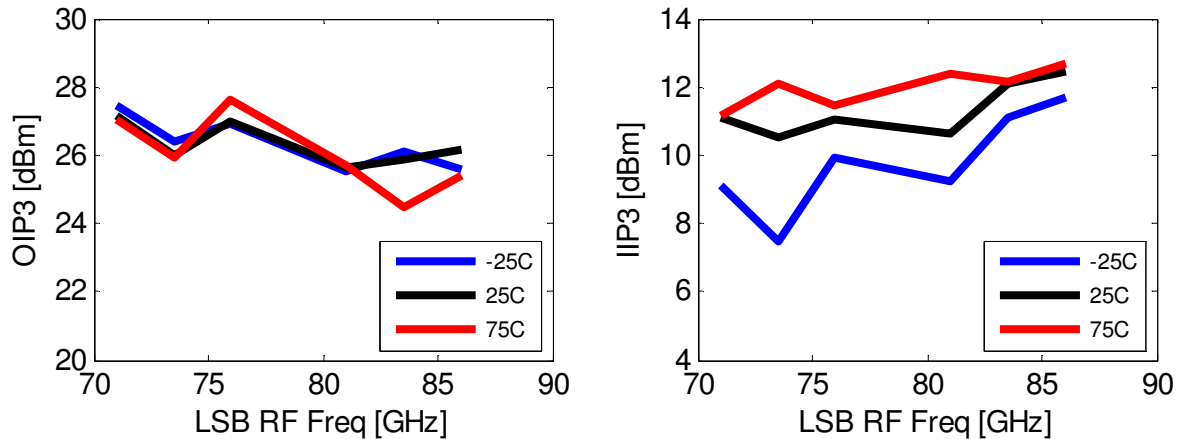


Figure 9. (Left): OIP3 vs frequency at maximum gain (ID1\_VGA + ID2\_VGA = 100 mA). (Right): IIP3 vs frequency measured at intermediate gain (ID1\_VGA + ID2\_VGA = 15 mA).

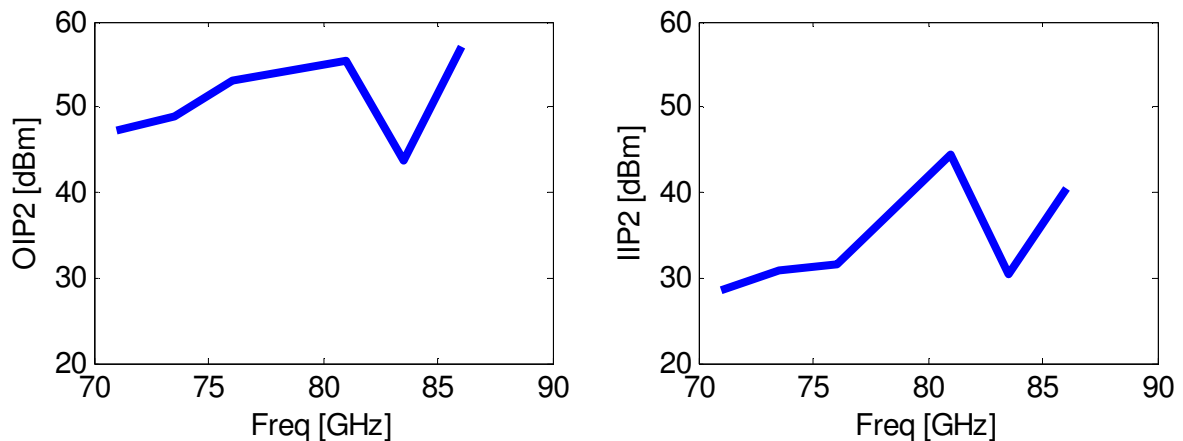


Figure 10. (Left): 2nd order intercept point (OIP2) at maximum gain (ID1\_VGA + ID2\_VGA is 100 mA). (Right): 2nd order intercept point (IIP2) at intermediate gain (ID1\_VGA + ID2\_VGA is 15 mA).

## RECOMMENDED OPERATING CONDITIONS

Bias should first be applied to the gates (VG...) followed by the drains (VD...). The gate voltages must be adjusted within the min/max range indicated in Table 3-Table 7 to obtain the specified drain currents. The drain currents are stated with all input signals off.

Table 3. Electrical settings on connector P1

Connector P1	Pad No.	Interface	I/O
GND	1		Ground
RF	2	$Z_0 = 50 \text{ Ohm}$ , AC coupled	Output
GND	3		Ground

Table 4. Electrical settings on connector P2

Connector P2	Pad No.	Bias settings (V/mA)			I/O
		Min	Typ <sup>[4]</sup>	Max	
VG1_VGA <sup>[5]</sup>	1	-1.2	-0.9	-0.4	Input
VD1_VGA <sup>[5]</sup>	2	3.2	3.3 / 7.5	3.4	Input
VG2_VGA <sup>[5]</sup>	3	-1.2	-0.9	-0.4	Input
VD2_VGA <sup>[5]</sup>	4	3.2	3.3 / 7.5	3.4	Input
VOUT_DET	5	0		VREF_DET	Output
VREF_DET	6		2.4		Output
GND	7				Ground
VG_DET	8	-1.1	-0.9	-0.7	Input
VD_DET	9	3.2	3.3 / <1	3.4	Input
VD1_PA	10	2.4	2.5 / 130	2.6	Input
VG1_PA	11	-0.5	-0.3	-0.1	Input
VG2_PA	12	-0.6	-0.4	-0.2	Input
VD2_PA	13	3.2	3.3 / 120	3.4	Input

<sup>[4]</sup> The gain is typically 12 dB when biasing the VGA at 15 mA (intermediate gain setting).

<sup>[5]</sup> Connect VG1\_VGA together with VG2\_VGA after a series 500 Ohm resistor on each gate. Connect VD1\_VGA together with VD2\_VGA.

**Table 5. Electrical settings on connector P3**

Connector P3	Pad No.	Interface	I/O
GND	1		Ground
LO	2	$Z_0 = 50 \text{ Ohm}$ , AC coupled	Input
GND	3		Ground

**Table 6. Electrical settings on connector P4**

Connector P4	Pad No.	Bias settings (V/mA)			I/O
		Min	Typ <sup>[4]</sup>	Max	
VG_MIX	1	-1.0	-0.8	-0.6	Input
VD_AMP	2	3.2	3.3 / 45	3.4	Input
VG_AMP	3	-0.6	-0.4	-0.2	Input
GND	4				Ground
VD_X2	5	3.2	3.3 / 10	3.4	Input
VD_X3	6	3.2	3.3 / 26	3.4	Input
VG_X2	7	-0.9	-0.8	-0.7	Input
VG_X3	8	-0.55	-0.45	-0.35	Input
NC	9				NC

**Table 7. Electrical settings on connector P5**

Connector P5	Pad No.	Interface	I/O
GND	1		Ground
Q+	2	$Z_0 = 100 \text{ Ohm}$ differential impedance, DC coupled	Input
Q-	3		Input
GND	4		Ground
I+	5	$Z_0 = 100 \text{ Ohm}$ differential impedance, DC coupled	Input
I-	6		Input
GND	7		Ground

## ABSOLUTE MAXIMUM RATINGS

Table 8. Absolute Maximum Ratings

Parameter	
Gate-source voltage	-2 to +0.7 V
Drain-source voltage	4.5 V
Gate-drain breakdown voltage	8 V
ID1_VGA, ID1_VGA	50 mA
ID1_PA, ID2_PA	200 mA
ID_AMP, ID_X2	80 mA
ID_X3	60 mA
IF in (I+, I-, Q+, Q-)	+7 dBm/ch.
IF in (I+, I-, Q+, Q-)	3 V <sub>pp</sub> /ch.
LO input power	+15 dBm
Operating temperature	-40 to + 85°C
Storage temperature	-65 to +150°C



## OUTLINE DRAWING

Mechanical drawing with pad locations is also available in dxf-file format on the web. The substrate thickness is 50  $\mu\text{m}$  (GaAs).

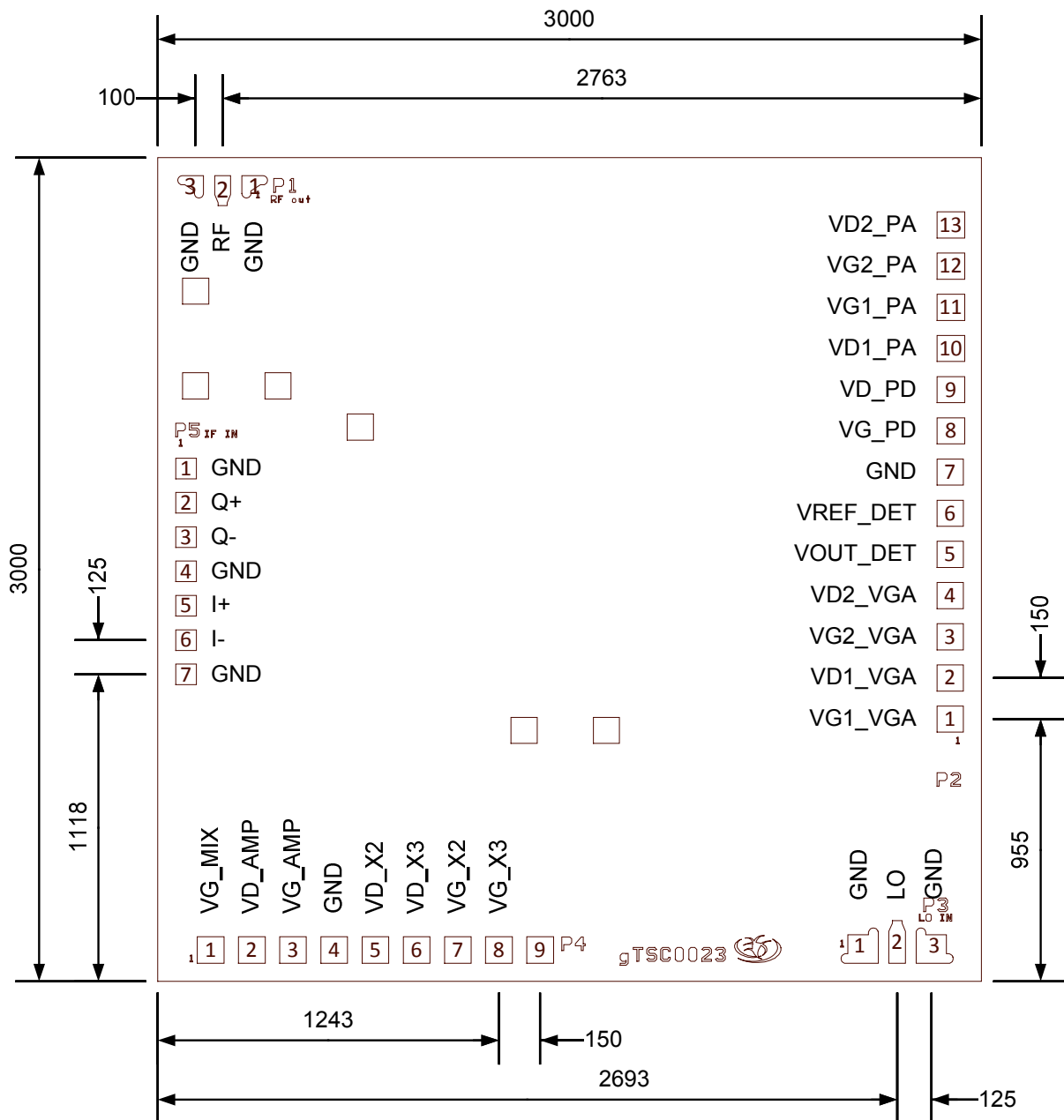


Figure 11. Outline drawing of the gTSC0023 MMIC. Dimensions are in  $\mu\text{m}$ .